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S-BAND GaAs POWER FET*

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ABSTRACT

The design, fabrication, and performance of an S-band GaAs power FET are described. A pulsed 38.4 mm gate width device has produced up to 20 W with 8 dB gain across the 3 to 3.5 GHz band.

INTRODUCTION

GaAs power FETs have been developed for phased-array radar applications at S-band. One program goal is a single stage amplifier having 25 W pulsed output power with 6 dB gain and 30% power-added efficiency across the 3.0 to 3.5 GHz band. The present paper discusses the design and fabrication of GaAs power FETs to meet these goals. The amplifier circuits used to match the device impedances are also described and the microwave performance of the devices in these circuits is presented.

DEVICE DEVELOPMENT

A number of tradeoffs must be made in designing a device to meet the performance goals of the previous paragraph. The most important factors are: total gate width, gate length, chip length, gate finger width, source lead inductance, device temperature rise, and device yield.

Although 1 W output power per mm gate width has been reported across a wide frequency range[1], this device is designed for about 2/3 W per mm in order to provide margin for less than optimum devices and for combining losses inherent in a large gate width device. The gate width chosen is 38.4 mm in 8 cells. A gate length of approximately 1.5 μm provides sufficient gain. The chip length is limited to 4 mm since larger chips would be difficult to handle and would be significantly larger than the circuit metallization width, causing unequal bond wire lengths to the different cells. A compromise between excessive chip length and gain degradation due to excesive gate finger width[2] is a gate finger width of 300 μm. A gate-to-gate spacing of about 20 μm is therefore necessary to fit all 128 gate fingers on the chip and to provide for source grounding (to be discussed shortly). In order to prevent excessive temperature rise with this close gate spacing it is necessary to employ a chip thickness of only 50 μm. Since this is too thin to handle easily, a thick plated heatsink is necessary.

A major device design problem is to reduce source lead inductance per unit gate width since excessive source lead inductance degrades gain. A device which has the parameters described above along with low source lead inductance is shown in Figure 1, a photograph of a slice during processing. Only four of the eight cells (19.2 mm gate width) are seen in the figure. The device is in the air bridge-via configuration in which a 25 μm x 250 μm via hole is etched through the GaAs

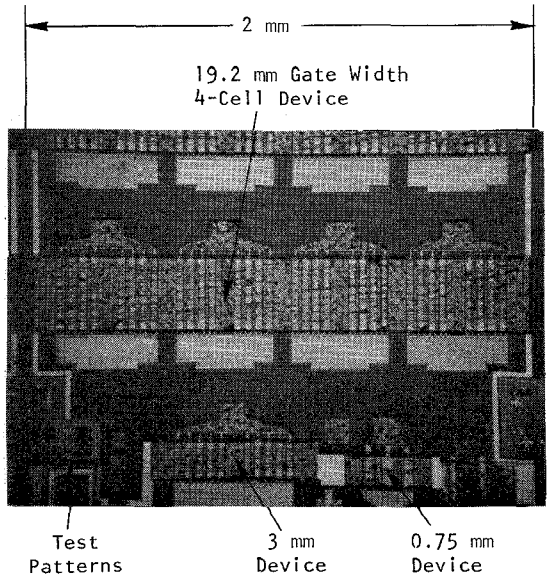

Figure 1. S-Band GaAs Power FET in Air Bridge-Via Configuration.

to the grounded plated heatsink at the extra wide source pads located after every eight gates (2400 μm gate width). The other source pads are connected to it by a plated gold air bridge covering most of the chip. By changing 3 photomasks the device can be fabricated in the topside-grounded configuration shown in Figure 2 in which sources are connected by plated Au air bridges to bonding areas along both sides of the chip. These are then bonded to ground. Also shown in Figures 1 and 2 are smaller gate width devices for lower power amplifier stages and several test patterns.

The device fabrication process is similar to that employed on other devices in our laboratory[3,4]. The active layers are grown by vapor-phase epitaxy on Cr-doped substrates grown by the Bridgman process. Two layers are grown sequentially using the Ga-$AsCl_3$-H_2 system: an undoped buffer layer 1 to 3 μm thick is followed by the sulfur-doped n-type active layer. The active layer is grown thicker than necessary (1 to 2 μm) and then thinned anodically. The devices are isolated by mesa etching and source and drain ohmic contacts are alloyed AuGe/Ni with a

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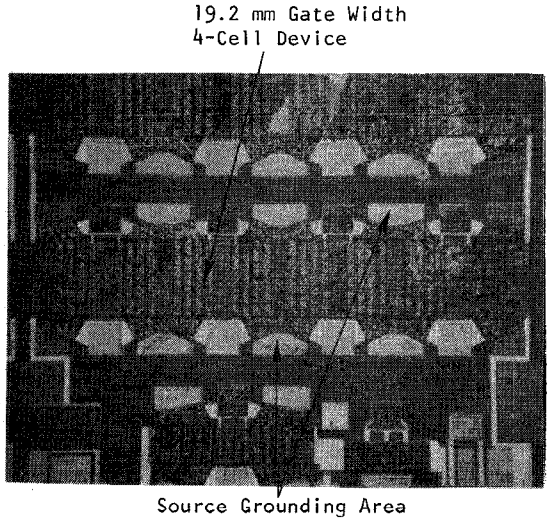

Figure 2. S-Band GaAs Power FET in Topside-Grounded Configuration.

6.25 μm separation. The gates are electron beam evaporated Ti/Pt/Au and are defined by contact printing or electron beam lithography. The slice is etched immediately prior to placing it in the evaporator in order to recess the gates ~ 0.1 μm below the epitaxial surface and reduce the device current to the correct value. A layer of Ti/Au is evaporated onto the slice to form the gate pads and source bonding areas in the topside-grounded configuration and also to increase the conductivity of the other contacts. The devices are protected with 0.4 μm of silicon nitride and the source air bridges are formed with 1-2 μm of plated gold which is also applied to all bonding pads. The slices are lapped and etched to 50 μm and the via holes are etched if required. Finally, 50 μm of gold is selectively plated to the back of the slice, interconnecting the vias if they are present, and the slice is sawed into chips.

Originally it was intended that all 38.4 mm be on a single plated heatsink. However, it was found that the differential thermal expansion of the GaAs and the plated heatsink cracked the GaAs during bonding. Therefore, the slices are now sawed into 19.2 mm gate width chips (2 mm long) which are mounted side-by-side and treated as a single chip for impedance matching purposes. An advantage of this procedure is that device yield is improved with the smaller chips.

Both device designs have produced good microwave performance and the air bridge-via devices don't require source bonds. However, the via etch process reduces yield. If the slice is not lapped very flat the chemically etched vias will be nonuniform with some devices shorted and others not contacted. Consequently, most slices have been in the topside-grounded configuration.

Good devices have been produced with both contact printed and e-beam defined gates. The device yield is much lower with optically-defined gates due to mask slice abrasion, mask-slice separation variations, and mask run-out. Consequently e-beam definition is used almost exclusively. A further advantage is that pattern changes are very easily implemented.

MICROWAVE PERFORMANCE

A critical part of obtaining good microwave performance from a GaAs FET with such a large gate width is to successfully match the extremely low input and output impedances to 50 Ω. A simple equivalent circuit model derived from small signal S-parameter measurements and modified for large signal operation was used for the impedance matching circuit design. Since a 38.4 mm gate width device has very low impedance, its S-parameters cannot be measured accurately so the values used are obtained by measuring smaller gate width devices (0.3 mm to 2.4 mm gate width) and scaling to 38.4 mm. The input impedance is insensitive to RF drive level but the output drain resistance must be reduced 50% from its small signal value to obtain the large signal value. The input impedance is approximately 0.2 Ω in series with 50 pF while the output impedance is 2.5 Ω in parallel with 9 pF. The impedance matching technique offering the most flexibility in matching the device over the necessary bandwidth is lumped element partial impedance matching. The matching circuit derived from the equivalent circuit parameters is shown in Figure 3 for a 38.4 mm gate width device. The

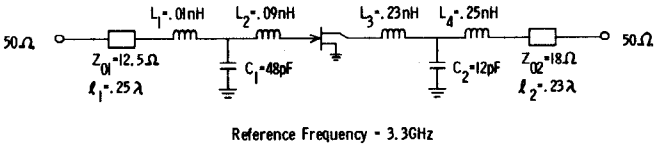

Figure 3. Matching Circuit Topology for 38.4 mm Gate Width FET at S-Band (2.8 to 3.8 GHz).

inductors and capacitors can, of course, be split up into several smaller capacitors with longer bond wires. Figure 4 shows the mounting configuration of a 38.4 mm gate width device (topside-grounded

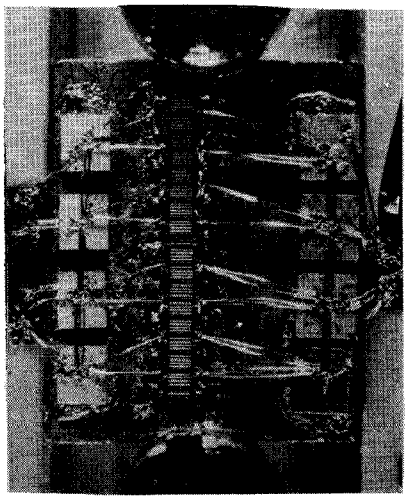

Figure 4. Mounting Configuration of a 38.4 mm Gate Width Device.

design). Two 19.2 mm gate width chips are used with four input matching capacitors having 12 pF each and four output matching capacitors of 3 pF each. The inductances are realized by gold bond wires. The FETs and capacitors are all mounted on a single gold-plated copper carrier which is screwed down to a holder containing the quarter wave transformers.

The CW output powers of 38.4 mm devices generally are in the range of 16 to 20 W with gains of 6 to 8 dB. The microwave performances of devices from several slices are listed in Table 1. The highest power reached was 20 W. It is interesting to note that devices from slice 80G-128-4 required 12 V drain bias to reach this power level but those from slice 80G-122-4 only required 10 V due to the higher doping level. This higher doping level also gave higher device gain. However, if doping level was increased further as with slice 81D1-23, performance decreased in spite of very good X-band performance (for a smaller device). From this data it is thought that the optimum doping level is in the range 5-10 x 10^{16} cm^{-3}. The highest gain for a 38.4 mm device is 8 dB and the highest efficiency is 40%. It should be noted that a 19.2 mm gate width device had 54% power-added efficiency, an exceptional value for a device this large. A device from slice 80G-126-4 was operated in a pulsed mode (drain pulsed) and the output power increased about 1 dB. Figure 5 shows the gain-frequency response of this amplifier which had 20 W output power with 8 dB gain.

CONCLUSIONS

A 38.4 mm gate width GaAs FET has been designed for S-band operation. It has been possible to operate such devices over the 3 to 3.5 GHz band using lumped element partial impedance matching. The best devices have had 20 W output power CW with 7 dB gain and 34% power-added efficiency. Other devices have had up to 8 dB gain and 40% efficiency at the 16 W power level. It is thought that 25 to 30 W output power will be obtained with similar gains and efficiencies after further device optimization.

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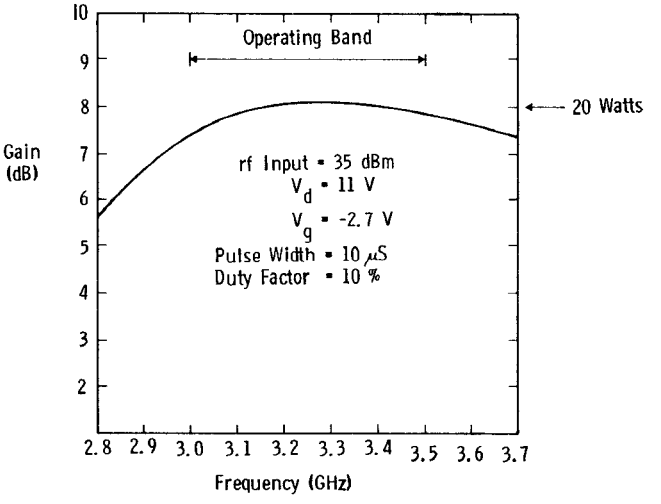

Figure 5. Gain-Frequency Response of a 38.4 mm Pulsed GaAs FET Amplifier.

TABLE 1 DEVICE MICROWAVE PERFORMANCE

Slice Number	Gate Width (mm)	CW Output Power (W)	Gain (dB)	Efficiency (%)	Drain Voltage (V)	Doping Level (X 10^{-16}) (cm^{-3})
80G-120-6	38.4	16	7	34	10	4-5
80G-134-8	19.2	10	9	54	8	6-7
81D1-23	38.4	15	5	30	8	18-19
80G-128-4	38.4	20	6	34	12	5-6
80G-120-4	38.4	16	7	31	8.5	8-9
80G-126-4	38.4	16	8	40	8.5	8-9
(Pulsed)		20	8	--	11	
80G-122-4	38.4	20	7	34	10	8-9